--1. **High-Performance, Superscalar-Based Computer System with Out-of-Order Instruction Execution**, Appl. No. 07/817,810, filed January 8, 1992, now U.S. Patent No. 5,539,911, by Le Trong Nguyen *et al.*;

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2. **High-Performance Superscalar-Based Computer System with Out-of-Order Instruction Execution and Concurrent Results Distribution**, Appl. No. 08/397,016, filed March 1, 1995, now U.S. Patent No. 5,560,032, by Quang Trang *et al.*;

3. **RISC Microprocessor Architecture with Isolated Architectural Dependencies**, Appl. No. 08/292,177, filed August 18, 1994, now abandoned, which is a FWC of Appl. No. 07/817,807, filed January 8, 1992, which is a continuation of Appl. No. 07/726,744, filed July 8, 1991, by Yoshiyuki Miyayama;

4. **RISC Microprocessor Architecture Implementing Fast Trap and Exception State**, Appl. No. 08/345,333, filed November 21, 1994, now U.S. Patent No. 5,481,685, by Quang Trang;

5. **Page Printer Controller Including a Single Chip Superscalar Microprocessor with Graphics Functional Units**, Appl. No. 08/267,646, filed June 28, 1994, now U.S. Patent No. 5,394,515, by Derek Lentz *et al.*, and

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6. **Microprocessor Architecture Capable with a Switch Network for Data Transfer Between Cache**, Memory Port, and IOU, Appl. No. 07/726,893, filed July 8, 1991, now U.S. Patent No. 5,440,752, by Derek Lentz *et al.*--

Page 2, please delete lines 1-11.

In the Claims

Please cancel claims 2-30 without prejudice or disclaimer.